Amendments to the Claims:

Please amend claims 1, 4, 5, 21, 24, and 25. Please cancel previously presented claims 3, 12-20, and 23, and add new claims 32-38. Following is a complete listing of the claims pending in the application, as amended:

1. (Currently Amended) A clock generator being applied to a DVD optical drive for generating a non-phase-modulated target clock signal based on a phase-modulated input signal, the clock generator comprising:

an arithmetic/logic circuit for calculating a period count value by counting a period of the input signal according to a reference clock having a predetermined frequency, calculating an average period value by averaging a plurality of the period count values, and comparing the average period value with the period count value for outputting a first control signal; and

a phase-locked loop connected to the arithmetic/logic circuit for generating the target signal according to the first control signal and the input signal, feeding the target signal back to the input of the phase-locked loop, and determining whether the target clock signal is to be synchronized with the input signal based on the logic level of the first control signal, the phase-locked loop comprising:

a phase-frequency detector connected to the arithmetic/logic circuit configured to generate a second control signal by comparing the target clock signal with the input signal and to determine whether the second control signal is outputted according to the logic level of the first control signal;

a loop filter connected to the phase-frequency detector configured to generate a control voltage based on the second control signal; and

a voltage-controlled oscillator connected to the loop filter configured to control the frequency of the target clock signal based on the control voltage;

wherein when the first control signal corresponds to a first logic level, the phase-locked loop compares the target clock signal with the input signal to drive the target clock signal to be synchronized with the input signal, and when the first control signal corresponds to a second logic level, the phase-locked loop holds the target clock signal without driving the target clock signal to be synchronized with the input signal.

2. (Previously Presented) The clock generator of claim 1, wherein the arithmetic/logic circuit comprises:

a reference clock generator for generating the reference clock having a predetermined frequency;

a counter connected to the reference clock generator for calculating the period count value by counting a period of the input signal according to the reference clock;

a mean operation unit connected to the counter for calculating an average period value by averaging a plurality of the period count values; and

a comparator connected to the counter and the mean operation unit for comparing the period count value with the average period value.

3. (Cancelled)

4. (Currently Amended) The clock generator of claim ~~3~~1, wherein the phase-locked loop further comprises a slicer connected to the phase-frequency detector and the voltage-controlled oscillator for slicing the target clock signal.

5. (Currently Amended) The clock generator of claim ~~3~~1, wherein the loop filter comprises a charge pump circuit for controlling the control voltage based on the second control signal.

6. (Previously Presented) The clock generator of claim 1, wherein when the difference between the period count value and the average period value is less than a critical value, the first control signal is set to a first logic level.

7. (Previously Presented) The clock generator of claim 1, wherein when the differences between a plurality of the consecutive period count values and the average period value are all less than a critical value, the first control signal is set to a first logic level.

8. (Previously Presented) The clock generator of claim 1, wherein when the difference between the period count value and the average period value is larger than a critical value, the first control signal is set to a second logic level.

9. (Previously Presented) The clock generator of claim 1, wherein when the differences between a plurality of the consecutive period count values and the average period value are all larger than a critical value, the first control signal is set to a second logic level.

10. (Previously Presented) The clock generator of claim 1, wherein the clock generator further comprises:

a band-pass filter for extracting the input signal having a frequency within a predetermined band; and

a slicer connected to the band-pass filter for slicing the input signal and forwarding the input signal to the arithmetic/logic circuit and the phase-locked loop.

11. (Previously Presented) The clock generator of claim 1, wherein the optical drive is a DVD-R optical drive or a DVD-RW optical drive, the optical drive comprising an ADIP decoder for predicting a timing for the input of the first period corresponding to

the next ADIP unit of the input signal and generating a second control signal to prohibit the phase-locked loop from driving the target clock signal to be synchronized with the input signal at a predetermined time before the timing of the input of the first period corresponding to the next ADIP unit of the input signal.

12-20. (Cancelled)

21. (Currently Amended) A clock generator being applied to a DVD optical drive for generating a non-phase-modulated target clock signal based on a phase-modulated input signal, the clock generator comprising:

a means for calculating a period count value by counting a period of the input signal according to a reference clock having a predetermined frequency, calculating an average period value by averaging a plurality of the period count values, and comparing the average period value with the period count value for outputting a first control signal; and

a means for generating the target signal according to the first control signal and the input signal, feeding the target signal back to the input of the means for generating the target signal, and determining whether the target clock signal is to be synchronized with the input signal based on the logic level of the first control signal, the means for generating the target signal comprising:

a means for generating a second control signal by comparing the target clock signal with the input signal, and for determining whether the second control signal is outputted according to the logic level of the first control signal;

a means for generating a control voltage based on the second control signal; and

a means for controlling the frequency of the target clock signal based on the control voltage;

wherein when the first control signal corresponds to a first logic level, the means for generating the target signal compares the target clock signal with the input signal to drive the target clock signal to be synchronized with the input signal, and when the first control signal corresponds to a second logic level, the means for generating the target signal holds the target clock signal without driving the target clock signal to be synchronized with the input signal.

22. (Previously Presented) The clock generator of claim 21, wherein the means for calculating a period count value comprises:

a means for generating the reference clock having a predetermined frequency;

a means for calculating the period count value by counting a period of the input signal according to the reference clock;

a means for calculating an average period value by averaging a plurality of the period count values; and

a means for comparing the period count value with the average period value.

23. (Cancelled)

24. (Currently Amended) The clock generator of claim ~~23~~21, wherein the means for generating the target signal further comprises a means for slicing the target clock signal.

25. (Currently Amended) The clock generator of claim ~~23~~21, wherein the means for generating a control voltage comprises a means for controlling the control voltage based on the second control signal.

26. (Previously Presented) The clock generator of claim 21, wherein when the difference between the period count value and the average period value is less than a critical value, the first control signal is set to a first logic level.

27. (Previously Presented) The clock generator of claim 21, wherein when the differences between a plurality of the consecutive period count values and the average period value are all less than a critical value, the first control signal is set to a first logic level.

28. (Previously Presented) The clock generator of claim 21, wherein when the difference between the period count value and the average period value is larger than a critical value, the first control signal is set to a second logic level.

29. (Previously Presented) The clock generator of claim 21, wherein when the differences between a plurality of the consecutive period count values and the average period value are all larger than a critical value, the first control signal is set to a second logic level.

30. (Previously Presented) The clock generator of claim 21, wherein the clock generator further comprises:

a means for extracting the input signal having a frequency within a predetermined band; and

a means for slicing the input signal and forwarding the input signal to the means for calculating a period count value and the means for generating the target signal.

31. (Previously Presented) The clock generator of claim 21, wherein the optical drive is a DVD-R optical drive or a DVD-RW optical drive, the optical drive comprising means for predicting a timing for the input of the first period corresponding to

the next ADIP unit of the input signal and generating a second control signal to prohibit the means for generating the target signal from driving the target clock signal to be synchronized with the input signal at a predetermined time before the timing of the input of the first period corresponding to the next ADIP unit of the input signal.

32. (New) A clock generating method being applied to a DVD optical drive for generating a non-phase-modulated target clock signal based on a phase-modulated input signal, the clock generating method comprising:

calculating a period count value by counting a period of the input signal according to a reference clock having a predetermined frequency;

calculating an average period value by averaging a plurality of the period count values;

comparing the average period value with the period count value;

outputting a first control signal based on the comparison;

comparing the target clock signal with the input signal;

generating a second control signal based on the first control signal and on the comparison of the target clock signal with the input signal; and

controlling the frequency of the target clock signal based on the second control signal;

wherein when the first control signal has a first logic level, the second control signal is generated to drive the target clock signal to be synchronized with the input signal and when the first control signal has a second logic level, the second control signal is generated to hold the target clock signal without driving the target clock signal to be synchronized with the input signal.

33. (New) The clock generating method of claim 32 further comprising:

initiating the average period count value with an initial value; and

calculating the average period count value by averaging a predetermined number of the period count values;

wherein when the average period value equals the initial value, the method further comprises stopping comparing the average period value with the period count value.

34. (New) The clock generating method of claim 32, wherein the outputting the first control signal comprises setting the first control signal to the second logic level when the difference between the period count value and the average period value is larger than a critical value.

35. (New) The clock generating method of claim 32, wherein the outputting the first control signal comprises setting first control signal to the second logic level when the differences between a plurality of the consecutive period count values and the average period value are all larger than a critical value.

36. (New) The clock generating method of claim 32, wherein outputting the first control signal comprises setting the first control signal to the first logic level when the difference between the period count value and the average period value is less than a critical value.

37. (New) The clock generating method of claim 32, wherein outputting the first control signal comprises setting the first control signal to the first logic level when the differences between a plurality of the consecutive period count values and the average period value are all less than a critical value.

38. (New) The clock generating method of claim 32, wherein the optical drive is a DVD-R optical drive or a DVD-RW optical drive, and the clock generating method further comprising predicting a timing for the input of the first period of the input signal and generating a second control signal for holding the target clock signal without driving

the target clock signal to be synchronized with the input signal at a predetermined time before the timing of the input of the first period of the input signal.